## What is claimed is:

[c1] 1.A rings-based system, comprising:
a plurality of ring members on a ring network that communicate using point-to-point connectivity;
a message traversing the ring from member to member;
the system being adapted so that upon the message arriving at a given ring member the message is processed by that ring member if the message is applicable to that ring member, and if the message is not applicable to that ring member, the message is passed on to the next ring member; and
a system clock signal for controlling timing on the ring network wherein the system clock signal is aligned between groups of ring members instead of among all of the ring members.

[c2] 2.The system of claim 1, wherein the system clock signal alignment is performed among adjacent ring members.

[c3] 3.The system of claim 2, wherein the alignment for a ring member is performed with respect to the ring member"s upstream and downstream ring member.

[c4] 4.The system of claim 1, wherein the system clock signal runs in the same direction as the message.

[c5] 5.The system of claim 1, wherein the system clock signal runs in the opposing direction to the message.

[c6] 6.The system of claim 1, wherein the alignment is performed by inserting logic at the ring members that ensures that the delay between adjacent clock signals does not exceed the delay between the adjacent members.

[c7] 7.The system of claim 1, wherein the alignment is performed using latches that are clocked by clock signals at individual members.

[c8] 8.The system of claim 1, further comprising a backpressure signal that runs in the opposing direction to the message, and wherein the alignment is performed by inserting logic at the ring members to ensure that the return path for the backpressure signal exceeds the clock delay between adjacent members.

[c9] 9.The system of claim 1, wherein the alignment substantially removes skew among the clock signals.

[c10] 10.The system of claim 1, wherein the alignment prevents a flip-flop at a ring member from sampling data a clock cycle too early.